PATENT
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In re Application of:

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Application No.:	Unassigned	Art Unit:	Unassigned
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For:	SEMICONDUCTOR INTEGRATED DEVICE		

CLAIMS PENDING AFTER PRELIMINARY AMENDMENT

1. A semiconductor integrated device comprising:

a first semiconductor device having a plurality of terminals; and

a second semiconductor device having a plurality of terminals, wherein at least some of the terminals of said first semiconductor device are connected with corresponding terminals of said second semiconductor device; and

a substrate on which said first and second semiconductor devices are mounted, wherein one group of terminals selected from the groups of terminals consisting of (i) the terminals of said first semiconductor device that are connected to corresponding terminals of said second semiconductor device, (ii) the terminals of said second semiconductor device that are connected to corresponding terminals of said second semiconductor device, and (iii) the terminals of said first and second semiconductor devices that are connected to each other, are commonly located.

2. The semiconductor integrated device according to claim 1, wherein terminals of said first and second semiconductor device that are connected to each other are arranged opposite each other on said substrate.

3. The semiconductor integrated device according to claim 1, wherein the groups of terminals selected from (i) the terminals of said first semiconductor device that are connected to the corresponding terminals of said second semiconductor device, (ii) the terminals of said second semiconductor device that are connected to the corresponding terminals of said second semiconductor device, and (iii) the terminals of said first and second semiconductor devices that are connected to each other, are located on one side of an edge part of said first and second semiconductor devices where the plurality of connecting terminals of said first semiconductor device or said second semiconductor device are located.

4. The semiconductor integrated device according to claim 1, wherein the groups of terminals selected from (i) the terminals of said first semiconductor device that are connected to the corresponding terminals of said second semiconductor device, (ii) the terminals of said second semiconductor device that are connected to the corresponding terminals of said second semiconductor device, and (iii) the terminals of said first and second semiconductor devices that are connected to each other, are arranged in series on a first side of an edge section of said first and second semiconductor devices where the plurality of connecting terminals of said first semiconductor device or said second semiconductor device are located and on a second side adjacent to the first side.

5. The semiconductor integrated device according to claim 1, wherein the connecting terminals of the group of terminals selected are arranged in series such that the connecting terminals are related, in order, to each other.

6. The semiconductor integrated device according to claim 1, wherein the respective pluralities of connecting terminals of said first semiconductor device and said second semiconductor device are arranged on a long side in a longitudinal direction of said first and second semiconductor devices, the respective short sides of said first semiconductor device and said second semiconductor device are arranged opposite to each other, and the connecting terminals of the selected group of

connecting terminals are arranged in series such that the groups are related with each other by, in order, from the short side in the long side, close to the short side.

7. The semi conductor integrated device according to claim 1, wherein said first semiconductor device comprises:

a power source input terminal which receives supply of a power source voltage from said second semiconductor device;

an oscillating unit connected to said power source input terminal and generating a signal with a frequency;

a multiplying unit which changes the frequency of the signal which said oscillating unit generates; and

an output terminal which outputs the signal; and

said second semiconductor device comprises:

a power source output terminal which supplies a power source voltage to said first semiconductor device; and

a signal input terminal which receives the signal from said output terminal.

8. A semiconductor integrated device according to claim 7, wherein said first semiconductor device further comprises:

a power source voltage supplying unit which supplies power to said oscillating unit; and

a power source switching unit which supplies power from the power source voltage supplying unit to said oscillating unit and said multiplying unit when said power source voltage supplying unit supplies power and which supplies power supplied from said power source input terminal to said oscillating unit and said multiplying unit when said power source voltage supplying unit does not supply power.

9. A semiconductor integrated device comprising:

a first semiconductor device having a plurality of terminals; and

a second semiconductor device having a plurality of terminals, wherein at least some of the terminals of said first semiconductor device are connected with corresponding terminals of said second semiconductor device; and

a substrate, having first and second sides, said first semiconductor device being mounted on the first side and said second semiconductor device being mounted on the second side, wherein one group of terminals selected from the groups of terminals consisting of (i) the terminals of said first semiconductor device that are connected to corresponding terminals of said second semiconductor device, (ii) the terminals of said second semiconductor device that are connected to the corresponding terminals of said second semiconductor device, and (iii) the terminals of said first and second semiconductor devices that are connected to each other, are located opposite each other, on the first and second sides of the substrate, and connected via respective through-holes in said substrate corresponding to and extending between the terminals.

10. The semiconductor integrated device according to claim 9, wherein the groups of terminals selected from (i) the terminals of said first semiconductor device that are connected to the corresponding terminals of said second semiconductor device, (ii) the terminals of said second semiconductor device that are connected to the corresponding terminals of said second semiconductor device, and (iii) the terminals of said first and second semiconductor devices that are connected to each other, are located on one side of an edge part of said first and second semiconductor devices where the plurality of connecting terminals of said first semiconductor device or said second semiconductor device are located.

11. The semiconductor integrated device according to claim 9, wherein the groups of terminals selected from (i) the terminals of said first semiconductor device that are connected to the corresponding terminals of said second semiconductor device, (ii) the terminals of said second semiconductor device that are connected to the corresponding terminals of said second semiconductor device, and (iii) the terminals of said first and

second semiconductor devices that are connected to each other, are arranged in series on a first side of an edge section of said first and second semiconductor devices where the plurality of connecting terminals of said first semiconductor device or said second semiconductor device are located and on a second side adjacent to the first side.

12. The semiconductor integrated device according to claim 9, wherein the connecting terminals of the group of terminals selected are arranged in series such that the connecting terminals are related, in order, to each other.

13. The semiconductor integrated device according to claim 9, wherein the respective pluralities of connecting terminals of said first semiconductor device and said second semiconductor device are arranged on a long side in a longitudinal direction of said first and second semiconductor devices, the respective short sides of said first semiconductor device and said second semiconductor device are arranged opposite to each other, and the connecting terminals of the selected group of connecting terminals are arranged in series such that the groups are related with each other by, in order, from the short side in the long side, close to the short side.

14. The semi conductor integrated device according to claim 9, wherein said first semiconductor device comprises:

a power source input terminal which receives supply of a power source voltage from said second semiconductor device;

an oscillating unit connected to said power source input terminal and generating a signal with a frequency;

a multiplying unit which changes the frequency of the signal which said oscillating unit generates; and

an output terminal which outputs the signal; and

said second semiconductor device comprises:

a power source output terminal which supplies a power source voltage to said first semiconductor device; and

a signal input terminal which receives the signal from said output terminal.

15. A semiconductor integrated device according to claim 14, wherein said first semiconductor device further comprises:

a power source voltage supplying unit which supplies power to said oscillating unit; and

a power source switching unit which supplies power from the power source voltage supplying unit to said oscillating unit and said multiplying unit when said power source voltage supplying unit supplies power and which supplies the power supplied from said power source input terminal to said oscillating unit and said multiplying unit when said power source voltage supplying unit does not supply power.